ABSTRACT OF THE DISCLOSURE

A semiconductor memory device comprises a plurality of memory cells each having a source terminal and a drain terminal and a ferroelectric capacitor having a first terminal connected to the source terminal, wherein the plurality of memory cells are connected in series, and one or more selected transistors connected to at least one terminal of the series connected memory cells to constitute a memory cell block, the memory cell block having one terminal connected to a bitline and another terminal connected to a plate electrode, and wherein two memory cell blocks, which are respectively connected to two bit lines forming a bit line pair and also connected to the same word line, are respectively connected to a first plate electrode and a second plate electrode.